***NAME :RAHUL GOEL***

***REG no: RA1911030010094***

***Section : O2***

***Date : 14/09/20***

EX\_9:HALF ADDER CIRCUIT

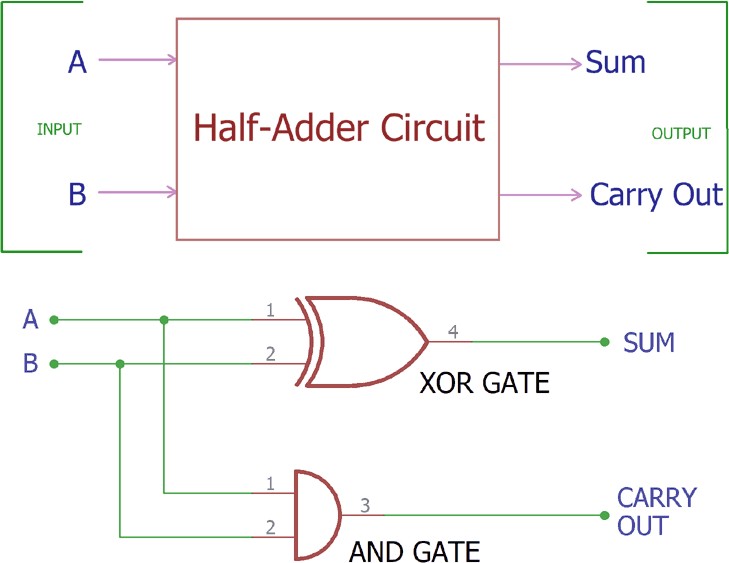
AIM: To design and implement a half adder circuit.

SOFTWARE USED: Logic gate simulator

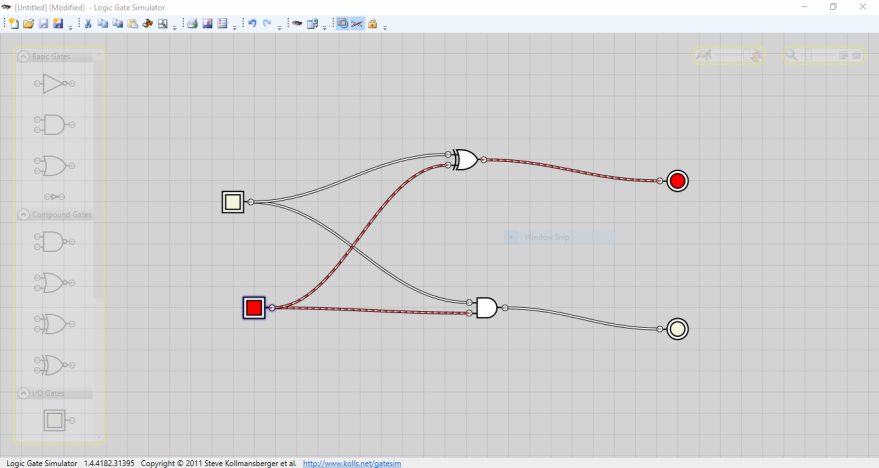
TRUTH TABLE:

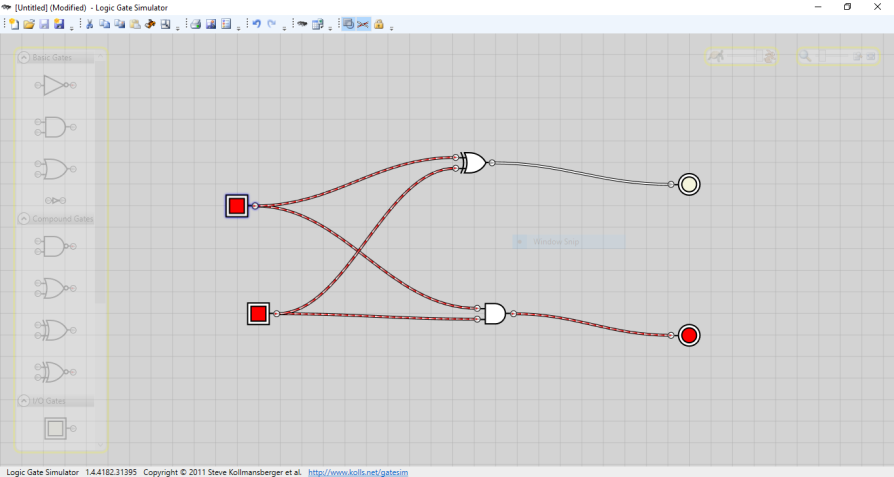
|  |  |  |  |
| --- | --- | --- | --- |
| Input | | outputs | |
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

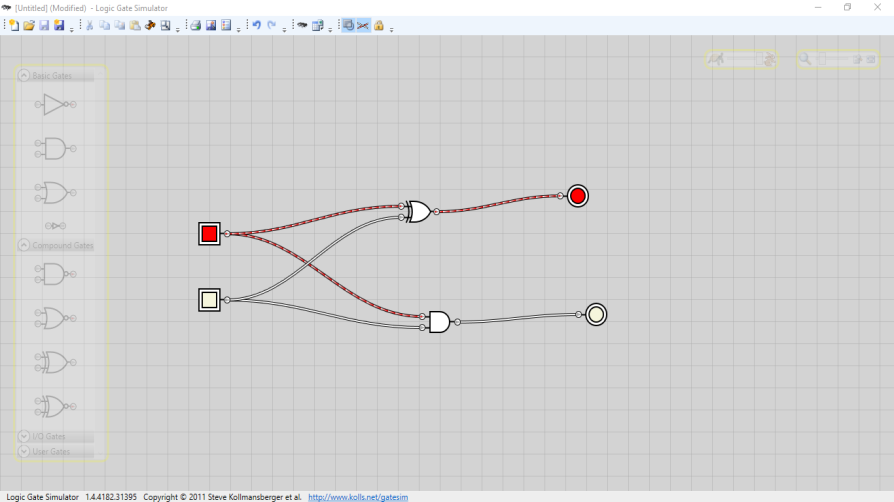
CIRCUIT DIAGRAM:

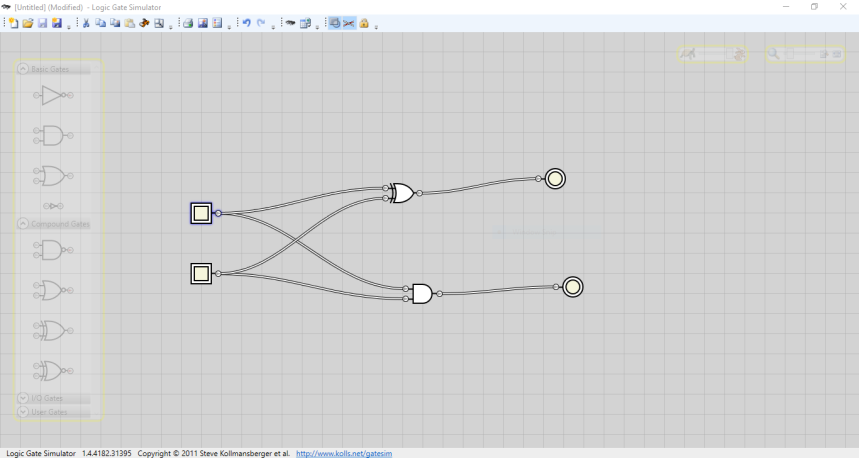


OUTPUT:









***RESULT: Here, we add two single digit binary numbers & results in two digit out.***